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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/909,736	07/19/2001	Young-Doo Jung	9903-19	2436

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EXAMINER
THAI, LUAN C

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/909,736	JUNG ET AL.	
	Examiner	Art Unit	
	Luan Thai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Abstract

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to ***a single paragraph*** on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim **9** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim **9**, the recitation "wherein inner leads to which both the first and the second link bonding wires are bonded are disposed at corners of the lead frame" is not

understood by the examiner. Particularly, since claim 8 defines that "first link bonding wires are connected between the electrode pads and the conductive pads and second link bonding wires connected between the conductive pads and the inner leads", how can inner leads have both the first and the second link bonding wires being connected to?

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> **(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.**

5. Claims 1, 3, 7-10 and 12-15, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Gow et al. (5,168,368).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3, 7-10 and 12-15, Gow et al. disclose a semiconductor chip package comprising: a semiconductor chip 10 having an active surface where a plurality of electrode pads 14 are formed; a lead frame having a plurality of leads 18; a plurality of bonding wires 27-28 electrically interconnecting the electrode pads 14 and corresponding leads 18; an encapsulant covering the chip, thereby forming a package body (Col. 1, lines

65+, Col. 3, lines 10+); the lead frame comprising: a die pad 13 on which the chip 10 is mounted; inner leads 18a-18n disposed around the die pad 13; a side ring pad 24 having plurality of metal pads 26 formed thereon, being disposed around the die pad and between the die pad 13 and the inner leads 18a-18n; a tie bar 13' (see figure 2) arranged to connect the die pad 13 and the side ring pad 24, wherein the bonding wires include first link bonding wires 27a-27n connected between the electrode pads 14a-14n and metal pads 26 and second link bonding wires 28a-28n connected between the metal pads 26 and the inner leads 18a-18n, and wherein the inner leads to which both the first and the second link bonding wires are bonded are disposed at corners of the lead frame. The claimed of "electrode pads including power electrode pads electrically connected to the side ring pad by power bonding wires" is taken to be inherent in the device package of Gow et al. since it apparent that some type of power electrode pads must present on the active surface of the semiconductor chip and being electrically connected to an external source (via power bonding wires—inner leads—outer leads) for the chip to function as intended.

6. Claims 1-3, 10 and 14-15, insofar as in compliance with 35 USC § 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Diffenderfer et al. (5,814,877).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-3, 10 and 14-15, Diffenderfer et al. disclose (see specifically figures 2, 3, 5, and 7) a semiconductor chip package comprising: a

semiconductor chip 2 having an active surface, wherein the claimed of a plurality of electrode pads being formed on active surface of the semiconductor chip is taken to be inherent in the device package of Diffenderfer et al. since bonding wires electrically connected between the chip and the leads are disclosed and it apparent that some type of electrode pads must exist on the active surface of the chip for the bonding wires electrically connected to. Diffenderfer et al. further disclose a lead frame having a plurality of leads 13; a plurality of bonding wires 10-11 electrically interconnecting the electrode pads of the chip and corresponding leads 13; an encapsulant 30 covering the chip, thereby forming a package body; the lead frame comprising: a die pad 3 on which the chip 2 is mounted; inner leads 13 disposed around the die pad 3; a power side ring pad 5 disposed around the die pad and between the die pad and the inner leads 13; a tie bar 7 arranged to connect the die pad 3 and the power side ring pad 5, wherein the die pad 3, the inner leads 13, and the tie bar are made of the same material (see figure 3), and a plurality of outer leads are made in one body with the plurality of inner leads (see figure 5); and wherein plurality of electrode pads formed on the semiconductor chip includes power electrode pads which are electrically connected to the power side ring pad 5 by power bonding wires 10 (see figure 7).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diffenderfer et al. (5,814,877) in view of Watanabe (5,365,106).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 4-6, Diffenderfer et al. disclose all the limitations of the claimed invention as detailed above except for the co-planarity of the chip and the inner leads 13. However, Diffenderfer et al. do state that the die bond pad 3 and thus the chip, which mounted thereon, may be downset via tie bar 7 (Col. 4, lines 44+) to accomplish certain other purposed (Col. 6, lines 17+). In addition, tie bars which include bent portions to arrange the co-planarity of the chip and the inner leads is conventional in semiconductor art, specifically in semiconductor lead frame art, as disclosed by Watanabe's figure 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the lead frame in Diffenderfer et al.'s device package to have the leads being coplanar with the chip, since such lead frame structure is conventional in semiconductor lead frame art, as disclosed by Watanabe's figure 1.

Regarding claim 11, Diffenderfer et al. disclose all the limitations of the claimed invention as detailed above except for the die pad having a bottom surface exposed from the package body.

Watanabe while related to a similar semiconductor lead frame package design teach the die pad 11a/21 having a bottom surface exposed from the package body 12/29 for realizing low thermal resistance (col. 1, lines 9+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Diffenderfer et al.'s device by forming the die pad to have a bottom surface exposed from the package body, as taught by Watanabe, for realizing low thermal resistance and for reducing the thickness of the package.

9. The following reference(s) is/are cited as of interest to this application:

U.S. Pat. No. 6,313,519 (figures 1-4) to Gainey et al. and U.S. Pat. No. 5,309,016 (figures 1, 2, 4, and 5) to Kasai et al. are cited for showing the tie bar includes a bent portion arranged to maintain the co-planarity of the chip and the inner leads.

In addition, U.S. Pat. No. 5,252,783 (figures 1-2) to Baird is cited for showing the tie bar includes a bent portion arranged to maintain the co-planarity of the chip and the inner leads, and the die pad having a bottom surface exposed from the package body.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone

numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
May 24, 2002

DAVID L. TALBOTT
SUPERVISORY PATENT EXAMINER
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